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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10069419	FILING DATE 04/12/2002	CLASS 335 400	SUBCLASS 492.000	GAU 2812	EXAMINER Harold Potts
**APPLICANTS: Fannasch Lothar; 8251					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A 371 OF PCT/DE00/02889 08/24/2000					
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** FOREIGN APPLICATIONS VERIFIED: GERMANY 199 40 480.1 08/26/1999					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO 048662-0129	
Verified and Acknowledged Examiners's initials					
TITLE : Conductor track supporting layer for laminating inside a chip card, chip card comprising a conductor track supporting layer, and method for producing a chip card					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	
ISSUE FEE		Total Claims	
Amount Due	Date Paid	Print Claim for O.G.	
		DRAWING	
		Sheets Drwg.	Figs.Drwg.
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	
		PREPARED FOR ISSUE	
		Application Examiner	
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